

The world's first Arbitrary Waveform Transceiver

Introducing Tabor's all new Proteus series, the world's first Arbitrary Waveform Transceiver. Based on a PXIe platform, the system integrates the ability to transmit, receive and perform digital signal processing all in a single instrument. The modular, compact and cost effective system offers industry leading performance, various configuration options, an innovative task oriented programming, and user programmable FPGA. So whether it is for aerospace and defense, telecommunications, automotive, medical or high-end physics applications Proteus opens the door to a world of infinite possibilities.

Leading Features:



Dual or Four channel 1.25GS/s & 2.5GS/s 16 bit, or Dual channel 9GS/s having 16 bit AWG & AWT configurations



Integrated NCO for digital upconverting to microwave frequencies



Real time data streaming directly to the FPGA for continuous and infinite waveform generation.



9GHz Bandwidth, 2.7GS/s 12 bit digitizer option for feedback control system and conditional waveform generation

Innovative task oriented sequence programming for maximum flexibility to generate any imaginable scenario

Up to 16GS/s waveform memory with the ability to simultaneously generate and download waveforms.

Excellent phase noise and spurious

performance

User customizable FPGA for demodulation. digital filtering and application specific



High speed

PCIe GEN3x8 lanes communication interface



Modular and space efficient PXI Express platform, easily scalable to hundreds of channels.



MODULE PLATFORM

ABOR ELECTRONICS



Modular, scalable and compact

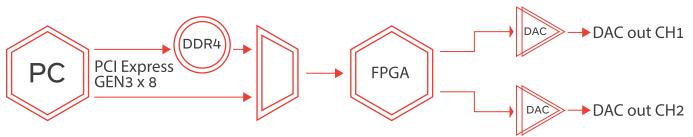
Based on PXI Express industry standard the modular architecture can easily scale to hundreds of channels, while keeping the required space to a minimum. The compact form size enables up to 4 generator output channels and 2 digitizer input channels to occupy only 3 PXI slots. So for synchronized, phase coherent, multi-channel applications such as quantum physics and radar applications the Proteus arbitrary waveform transceiver is an ideal, space efficient and cost effective solution.

Ultra-fast communication interface

Spending more time setting up your generated scenario than actually running it? The PCI Express Gen 3 x8 lanes connection enables up to 64Gb/s of data transfer speed. This enables the Proteus arbitrary waveform transceiver to offer the fastest waveform download available on the market today, saving you one of your most valuable resources, time.

Feedback control system

Many of today's applications, require conditional waveform generation depending on input signals from the environment. The Proteus arbitrary waveform transceiver flawlessly integrates both DAC and ADC in one system, controlled by a single FPGA for optimal synchronization and minimum latency. This high speed control system provides a feedback loop for fast decision making on the fly with minimum latency.



Generate any imaginable scenario

The new series offers an innovative task oriented sequence programming where user can change the full instrument set up at every line of the task table. In addition, not only can users of the Proteus series instruments generate and download waveforms simultaneously, they can stream data directly to the FPGA without the need to use the built in memory. This enables generating random, unique and infinitely long scenarios directly from the controlling PC at DAC speeds of up to 9GS/s. So no matter whether your scenario is extremely complex, infinite or even dynamic you can generate it with the Proteus series model



GENERAL CHARACTERISTICS	P9082M	P2582M	P2584M	P1282M	P1284M
MAX. SAMPLE RATE	9GS/s	9GS/s 2.5GS/s 1.25GS/s			
RESOLUTION		16-bit ⁽¹⁾			
ENOB AT MAX. FREQUENCY		TBD			
NUMBER OF CHANNELS	2	2	4	2	4
BANDWIDTH	9GHz ⁽²⁾ 4.5GHz ⁽³⁾	5GHz ⁽²⁾ 2.5GHz ⁽²⁾ 2.5GHz ⁽³⁾ 1.25GHz ⁽³⁾			
MEMORY	Up to 16GS	Up to 8GS Up to 4GS		4GS	
INTERFACE		PXI Express Gen.3 x8 lanes			
LATENCY / SYSTEM DELAY		200ns			
FINE DELAY		-5ns to 5ns			
DELAY RESOLUTION		5ps resolution			
COARSE DELAY		0 to wavelength in 1 sample point resolution			
INITIAL SKEW BETWEEN CHANNELS		Ops			

(1) Depending on sampling mode (2) Direct output option (3) DC output option

ARBITRARY / TASK TABLE	P9082M	P2582M	P2584M	P1282M	P1284M
MINIMUM SEGMENT LENGTH NORMAL FAST SEGMENT	2048 points1024 points128 points64 points		1024 p 64 po		
WAVEFORM GRANULARITY STANDARD OPTIONAL	64 points 32 points 32 points 16 points			32 points 16 points	
SEGMENTS	2^15				
SEGMENT LOOPS	2^20				
SEQUENCES	2^15				
SEQUENCE TABLE ENTRIES	2^15				
SEQUENCE LOOPS	2^20				
ADVANCED SEQUENCES TABLE ENTRIES	1024				

SIGNAL PURITY	DC OUTPUT	DIRECT OUTPUT		
HARMONIC DISTORTION				
fout = 100 MHz	<-75 dBc (typ)	<-80 dBc (typ)		
fout = 10 MHz - 500 MHz, DC to 2 GHz	<-70 dBc (typ)	<-75 dBc (typ)		
fout = 10 MHz 3 GHz, DC to 4.5 GHz	<-65 dBc (typ)	<-70 dBc (typ)		
fout = 10 MHz 7 GHz, 5 to 10 GHz		TBD		
SFDR				
fout = 10 MHz1 GHz DC to 1 GHz	-85 dBc (typ)	<-85 dBc (typ)		
fout = 1 GHz3 GHz , DC to 3 GHz	-75 dBc (typ	<-75 dBc (typ)		
fout = 3 GHz4.5 GHz , DC to 4.5 GHz	-65 dBc (typ)	<-65 dBc (typ)		
fout = 3 GHz4.5 GHz , DC to 4.5 GHz	100us Full bandwidth	-<70 dBc (typ)		
fout = 7 GHz, 6 to 8 GHz (2nd Nyquist)	<6us Narrow bandwidth (<10% BW) -<70 dBc (typ)			
PHASE NOISE (@10kHz offset)				
fout = 187.5MHz	-130 dE	-130 dBc/Hz		
fout = 375MHz	-125 dBc/Hz			
fout = 750MHz	-120 dBc/Hz			
fout = 2GHz – 5GHz	-110 dBc/Hz			
fout = 5GHz - 7GHz	-105 dBc/Hz			



TABOR ELECTRONICS



DC OUTPUT		DIRECT OUTPUT (OPTIONAL)		
OUTPUT TYPE	Single-ended or differential, DC-coupled	OUTPUT TYPE	Single-ended or differential, AC coupled	
IMPEDANCE	50 Ω (nom)	IMPEDANCE	50 Ω (nom)	
AMPLITUDE	100 mVp-p to 1.2 Vp-p	AMPLITUDE	600mVpp,	
AMPLITUDE RESOLUTION	±(3% of amplitude ±2 mV)		single-ended into 50 Ω	
VOLTAGE WINDOW	±2V	AMPLITUDE RESOLUTION	1mV	
OFFSET RESOLUTION	1mV	AMPLITUDE ACCURACY	±(3% of amplitude ±2 mV)	
DC OFFSET ACCURACY	\pm (2.0% of offset \pm 10 mV)	BANDWIDTH		
SKEW BETWEEN NORMAL AND COMPLEMENT OUTPUTS	0 ps	-3dB analog BW 2ND Nyquist zone BW	100 kHz to 4.5 GHz (typ) Up to 9GHz	
RISE/FALL TIME (20% TO 80%)	<150 ps (typ)	CONNECTOR TYPE	SMA	
JITTER (PEAK-PEAK)	<15 ps (typ)	REFERENCE CLOCK OUTPUT		
OVERSHOOT	<5% (typ)	FREQUENCY	10MHz / 100MHz selectable	
CONNECTOR TYPE	SMA	CONNECTOR	SMP	

MARKER OUTPUTS	P9082M	P2582M	P2584M	P1282M	P1284M	
NUMBER OF MARKERS	8	8	8	4	4	
OUTPUT TYPE	Single Ended					
OUTPUT IMPEDANCE		50 Ω (nom)				
LEVEL		100 mVp-p to 1.2 Vp-p with 40mV resolution				
RISE/FALL TIME (20% TO 80%)	<400ps					
MARKER TO DIRECT/DC OUT	<1SCLK					
WIDTH	User defined, in points					
DELAY CONTROL	Position control in points					
RANGE	0 - waveform length					
RESOLUTION	8 points 2 points					
CONNECTOR TYPE	SMP					

SYNC CLOCK OUTPUT		SAMPLE CLOCK OUTPUT	
FREQUENCY	1/64 of the sample clock frequency	SOURCE	Selectable, internal synthesizer or sample clock input
CONNECTOR	SMP	FREQUENCY RANGE	SCLK Range
SAMPLE CLOCK OUTPUT		OUTPUT AMPLITUDE	400 mVpp (nom), fix
SAMPLE CLOCK OUTPUT		INPUT IMPEDANCE	50 Ω (nom), AC coupled
SOURCE	Selectable, internal synthesizer or sample clock input	AMPLITUDE ACCURACY	±(3% of amplitude ±2 mV)
FREQUENCY RANGE	SCLK Range	TRANSITION TIME (20% TO 80%)	20 ps (typ)
OUTPUT AMPLITUDE	400 mVpp (nom), fix	CONNECTOR	CNAA
INPUT IMPEDANCE	50 Ω (nom), AC coupled	CONNECTOR	SMA
AMPLITUDE ACCURACY	±(3% of amplitude ±2 mV)		
TRANSITION TIME (20% TO 80%)	20 ps (typ)		
CONNECTOR	SMA		





FAST SEGMENT DYNAMIC CONTROL	_ INPUT (OPTIONAL)
NUMBER OF ADDRESSABLE SEGMENTS OR SEQUENCES	256
DATA RATE	TBD
SET-UP TIME	TBD
HOLD TIME	TBD
INPUT RANGE LOW LEVEL HIGH LEVEL	0 V to +0.7 V +1.6 V to +3.6 V
IMPEDANCE	TBD
CONNECTOR	TBD
REFERENCE CLOCK INPUT	
INPUT FREQUENCIES	10MHz / 100MHz selectable
LOCK RANGE	± 1MHz
INPUT LEVEL	0.2 Vp-p to 3.0 Vp-p
IMPEDANCE	50 Ω , AC coupled (nom)
CONNECTOR TYPE	SMP
SAMPLE CLOCK INPUT	
FREQUENCY RANGE	SCLK Range
INPUT POWER RANGE	+0 dBm to +7 dBm
DAMAGE LEVEL	+8 dBm
INPUT IMPEDANCE	50 Ω nom, AC coupled
CONNECTOR TYPE	SMA

GENERAL	
Interface:	PXIe Gen3 x8 Lanes
Power Consumption:	50W max per slot
Current Consumption:	+3.3V 4A max. +12V 4A max.
Dimensions:	Base – 8HP PXIe (2 Slots)
With Options:	12HP PXIe (3 Slots)
Weight: Without Package Shipping WeightApprox.	Approx. 1 Kg 1.5 Kg
Temperature: Operating Storage	0°C to +40°C -40°C to +70°C
Warm up time:	15 minutes
Humidity:	85% RH, non-condensing
Safety:	CE Marked, EC61010-1:2010
EMC:	IEC 61326-1:2013
Calibration:	2 years
Warranty:	1/3year warranty plan

TRIGGER/GATE AND EVENT INPUT		
INPUT RANGE	±5 V	
THRESHOLD RANGE RESOLUTION SENSITIVITY	–5 V to +5 V 100 mV 200 mV	
JITTER @ MAX CLOCK	3.2ns (200ps optional)	
POLARITY	Pos or Neg	
DRIVE	Selectable channel 1, channel 2 or both	
INPUT IMPEDANCE	1 k or 50 Ω (nom), DC coupled	
MAX TOGGLE FREQUENCY	TBD	
MINIMUM PULSE WIDTH	TBD	
CONNECTOR TYPE	SMP	

ORDERIN	G INFORMATION
MODEL	DESCRIPTION
P1282M	PXIe 1.25GS/s, 16Bit, AWG, 1GS Memory, 2CH, 4 Markers
P1284M	PXIe 1.25GS/s, 16Bit, AWG, 1GS Memory, 4CH, 4 Markers
P2582M	PXIe 2.5GS/s, 16Bit, AWG, 1GS Memory, 2CH,8 Markers
P2584M	PXIe 2.5GS/s, 16Bit, AWG, 1GS Memory, 4CH, 8 Markers
P9082M	PXIe 9GS/s, 16 Bit AWG, 4GS Memory, 2CH, 8 Markers
OPTION	DESCRIPTION
4M1	4GS Memory option for models P1282Mand P2582M
4M2	4GS Memory option for models P1284M and P2584M
8M1	8GS Memory option for models P1282Mand P2582M
8M2	8GS Memory option for models P1284M, P2584M and P9082M
16M1	16GS Memory option for models P9082M
DO1	9GHz BW Direct Output option for models P1282M and P2582M
DO2	9GHz BW Direct Output Opt. for models P1284M, P2584M & P9082M
FS1	Fast Segment Control option for models P1282M & P2582M
FS2	Fast Segment Control Opt. for models P1284M, P2584M & P9082M
MRK1	x8 Extra Markers option for models P1282M & P2582M
MRK2	x8 Extra Markers Opt. for models P1284M, P2584M & P9082M
LTJ1	Ultra Low Trigger Jitter (200ps typ.) Opt. for models P1282M &P2582M
LTJ2	Ultra Low Trigger Jitter (200ps typ.) Opt. for models P1284M, P2584M & P9082M
G1	Low Waveform Granularity Opt. for models P1282M & P2582M
G2	Low Waveform Granularity Opt. for models P1284M, P2584M & P9082M
AWT1	9GHz BW, 2.7GS/s 12 Bit 1CH Digitizer option for models P128xx & P258xx & P9082x
FPGA PROG	FPGA Programming capability with high level code through decision blocks
FPGA Shell	FPGA full control & programming











